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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,707	11/09/2001	Ken Jaramillo	101950.00076	5641

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EXAMINER	
LEE, CHRISTOPHER E	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 08/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,707	JARAMILLO ET AL.	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4 and 6-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4 and 6-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 November 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the request filed on 15th of August 2005 for a Request for Continued Examination (RCE) under 37 CFR 1.114 based on the Application No.10/039,707, which the request is acceptable and an RCE has been established. Claim 1 has been amended; claims 3 and 5 have been canceled; and no claim has been newly added since the Final Office Action was mailed on 10th of February 2005. Currently, claims 1, 2, 4 and 6-19 are pending in this Application.

Specification

2. Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

In this case, the abstract refers to purported merits, such that "Advantageously, the bridge (350) responds to the memory read multiple command differently than either the memory read or the memory read line command" on the specification, page 24, lines 14-16. See MPEP 608.01(b).

Drawings

3. Figure 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated in the Application, page 5, lines 11-12, and page 13, lines 17-18. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the claimed subject matter "second bus has cache memory" in line 10 of the claim 1 must be shown or the feature canceled from the claim. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Notice of Claim Renumbering under Rule 37 CFR 1.126

5. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not). Misnumbered claims 19 and 20 have been renumbered 18 and 19, respectively.

Duplicate Claim Warning

6. Applicant is advised that should claim 12 be found allowable, claim 14 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Objections

7. The claim 1 recites the limitation "the amount of data prefetched by the memory read multiple command" in line 8. However, the subject matter "the amount" has not been specifically clarified in the claim. Therefore, the Examiner presumes that the term "the amount" could be considered as --an amount -- in light of the specification since it is not defined in the claims.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

9. Claims 13 is rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for using the memory read multiple command in an attempt by a SCSI disk controller 210 (initiator), which is coupled to a secondary PCI bus 215, to read large amounts of data from system

memory 220 (target), which is coupled to primary PCI bus 240 via a host bridge 230 in Fig. 2 (See Application, page 13, line 19 through page 14, line 11), does not reasonably provide enablement for adapting the second bus, which is coupled to a target (i.e., system memory 220 of Fig. 2; See Claim 1, lines 4-6, in fact, the first bus should be coupled to the initiator, and the second bus should be coupled to the target), to support the SCSI disk controller as an initiator because the initiator should be coupled to the first bus in light of the specification. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make/use the invention commensurate in scope with these claims. The Examiner doubt how the subject matter "SCSI disk controller" is adapted to the subject matter "the second bus" under the limitation "the bridge adapted to perform memory read, memory read line, and memory read multiple commands from the first to the second bus" (See Claim 1, lines 4-6). In other words, the subject matter "SCSI disk controller" could not be adapted to the subject matter "the second bus" since the SCSI disk controller is not a target, but an initiator in light of the specification (See Figs. 2 and 3).Therefore, the term "the second bus" could be considered as --the first bus -- since it is clearly defined in the specification for the purpose of the claim rejection based on a prior art.

Claim Rejections - 35 USC § 102

10. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

11. Claim 15 is rejected under 35 U.S.C. 102(b) as being anticipated by Corrigan et al. [US 5,983,306 A ; hereinafter Corrigan].

Referring to claim 15, Corrigan discloses a controller apparatus (i.e., Bridge Circuit in Fig. 1), comprising:

- a first bus (i.e., Secondary I/O Bus 3 of Fig. 2) adapted to facilitate data transfer (i.e., for data transferring between Secondary Bus Master 30 and PCI bus bridge 1 in Fig. 1);

- a second bus (i.e., Primary I/O Bus 4 of Fig. 2) adapted to facilitate data transfer (i.e., for data transferring between Primary Bus Slaves 40, 50, 60 and PCI bus bridge 1 in Fig. 1; See col. 5, lines 1-4); and
- a controller (i.e., PCI bus bridge 1 of Fig. 2) coupling said first bus to said second bus (See col. 4, line 67 through col. 5, line 1),
    - said controller adapted to perform memory read, memory read line, and memory read multiple commands (See col. 3, lines 31-57) from said first bus (i.e., Secondary I/O Bus as an initiator) to said second bus (i.e., Primary I/O Bus as a target; See col. 5, lines 12-14).

12. Claims 16-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Peters et al. [US 6,636,927 B1; hereinafter Peters].

Referring to claim 16, Peters discloses a method of operating (See Abstract and Fig. 5) a bridge (i.e., PCI-to-PCI Bridge 216 in Fig. 2) coupled between a first bus (i.e., Secondary PCI bus 218 of Fig. 2) and a second bus (i.e., Primary PCI bus 204 of Fig. 2; See col. 6, lines 10-14), comprising:

- initiating a read multiple command on said first bus (See col. 6, lines 37-43);
- said bridge passing said read multiple command to a target (i.e., selected slave device, e.g., Main Memory (RAM) 214 of Fig. 2) on said second bus (See col. 6, lines 43-47), wherein
    - said bridge (i.e., PCI-to-PCI Bridge) also supports a memory read and a memory read line command (See col. 10, lines 30-64); and
    - said bridge treating said read multiple command differently than said memory read line command (See Fig. 6 and col. 9, lines 20-44; i.e., PCI-to-PCI Bridge treats read multiple command with a fetch size in F2 field of a prefetch control register differently than memory read line command with a fetch size in F1 field of the prefetch control register).

Referring to claim 17, Peters teaches

- said bridge (i.e., PCI-to-PCI Bridge 216 in Fig. 2) prefetches more data in response to said memory read multiple command than that prefetched in response to a memory read command (See col. 9, lines 32-40; i.e., memory read multiple command prefetches multiple memory cache lines from a memory. However, memory read command prefetches only less than a cache line from the memory).

Referring to claim 18, Peters discloses a controller (i.e., RAID Controller 206 in Fig. 2) adapted to prefetch data via a first bus (i.e., Secondary PCI bus 218 of Fig. 2) from a target (i.e., selected slave device, e.g., Main Memory (RAM) 214 of Fig. 2) on a second bus (i.e., Primary PCI bus 204 of Fig. 2; See col. 3, lines 31-57), comprising

- a circuit (i.e., PCI-to-PCI Bridge 216 in Fig. 2) adapted to respond to a memory read multiple command and a memory read line command (See col. 10, lines 30-64),
- whereby said circuit prefetches more data from said target in response to said memory read multiple command than said memory read command (See col. 9, lines 32-44).

However, the recitation in the claim "whereby the circuit prefetches more data from the target in response to the memory read multiple command than the memory read command" has not been given patentable weight because it has been held that the functional "whereby" statement does not define any structure and accordingly cannot serve to distinguish. *In re Mason, 114 USPQ 127, 44 CCPA 937 (1957).*

Referring to claim 19, Peters teaches

- said circuit (i.e., PCI-to-PCI Bridge 216 in Fig. 2) prefetches more data from said target (i.e., selected slave device, e.g., Main Memory (RAM) 214 of Fig. 2) in response to said memory read

multiple command than said memory read line command (See col. 9, lines 34-40; i.e., memory read multiple command prefetches multiple memory cache lines from a memory. However, memory read line command prefetches only one complete cache line from the memory).

Claim Rejections - 35 USC § 103

13. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

14. Claims 1, 2, 4, 6-9, and 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peters et al. [US 6,636,927 B1; hereinafter Peters] in view of AAPA [Applicants' Admitted Prior Art].

Referring to claim 1, Peters discloses a bridge apparatus (i.e., RAID Controller 206 in Fig. 2), comprising:

- a first bus (i.e., Secondary PCI bus 218 of Fig. 2) adapted to facilitate data transfer (See col. 7, lines 37-38);
- a second bus (i.e., Primary PCI bus 204 of Fig. 2) adapted to facilitate data transfer (See col. 5, lines 52-54);
- a bridge (i.e., PCI-to-PCI Bridge 216 in Fig. 2) coupling said first bus to said second bus (See col. 6, lines 10-14),
    - said bridge adapted to perform memory read, memory read line, and memory read multiple commands from said first bus to said second bus (See col. 10, lines 30-64),
        - wherein said bridge (i.e., PCI-to-PCI Bridge) responds to said memory read multiple command differently than either said memory read or said memory read line command (See Fig. 6 and col. 9, lines 20-44; i.e., PCI-to-PCI Bridge responds to memory read multiple command with a fetch size in F2 field of a prefetch control register differently than either memory read with a fetch size in

F0 field of the prefetch control register or memory read line command with a fetch size in F1 field of the prefetch control register);

- wherein an amount of data prefetched by said memory read multiple command is selectively variable in size (See col. 3, lines 45-57 and col. 9, lines 37-40; in fact, F2 field value, viz., amount of data prefetched, in prefetch control register 308 is selectively set variable in size by master device).

Peters does not expressly teach second bus having cache memory, wherein said bridge apparatus is adapted to perform memory read multiple command with said cache memory.

AAPA discloses a conventional PCI to PCI bridge handling a memory read multiple command (Fig. 2), wherein

- a second bus (i.e., Primary PCI Bus 240 of Fig. 1) has cache memory (See page 9, lines 1-3; i.e., wherein in fact that memory read multiple cycles are used typically when a device is accessing Cache memory implies that a second bus has cache memory), and
- a bridge apparatus (i.e., PCI to PCI bridge 250 and Primary/Secondary PCI Busses 215, 240 in Fig. 2) is adapted to perform memory read multiple command with said cache memory (See page 13, line 16 through page 14, line 11).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said means for handling said memory read multiple command, as disclosed by AAPA, to said bridge apparatus, as disclosed by Peters, for the advantage of offering much higher read performance for high end system (See AAPA, page 9, lines 11-13).

Referring to claim 2, Peters teaches

- said memory read multiple command prefetches more data than said memory read command (See col. 9, lines 32-40; i.e., memory read multiple command prefetches multiple memory cache lines

from a memory. However, memory read command prefetches only less than a cache line from the memory).

Referring to claim 4, Peters teaches

- said memory read multiple command prefetches more data than said memory read line command (See col. 9, lines 34-40; i.e., memory read multiple command prefetches multiple memory cache lines from a memory. However, memory read line command prefetches only one complete cache line from the memory).

Referring to claim 6, Peters teaches

- second bus (i.e., Primary PCI bus 204 of Fig. 2) has RAM memory (i.e., Main Memory (RAM) 214 of Fig. 2),
    - wherein said bridge apparatus (i.e., RAID Controller 206 in Fig. 2) is adapted to perform memory read multiple command with said RAM memory (See col. 6, lines 31-47).

Referring to claim 7, AAPA teaches

- said bridge (i.e., Host Bridge 230 in Fig. 2) having a prefetch buffer (i.e., Prefetch Buffer 232 of Fig. 2), wherein
    - said prefetch buffer is adapted to be flushed after a memory read multiple command by said first bus (i.e., Primary PCI Bus 240 of Fig. 2; See page 14, lines 9-11).

Referring to claims 8 and 9, Peters teaches

- said memory read multiple command utilizes at least 64 Dwords (See col. 9, lines 56-67; i.e., memory read multiple command utilizes a read prefetch buffers 702 in segment of which the size is 256 bytes, viz., 64 double words in Fig. 7).

Referring to claim 11, Peters teaches

- said first bus (i.e., Secondary PCI bus 218 of Fig. 2) is a PCI bus.

Referring to claims 12 and 14, Peters teaches

- said second bus (i.e., Primary PCI bus 204 of Fig. 2) is a PCI bus.

Referring to claim 13, Peters teaches

- said first bus (i.e., Secondary PCI bus 218 of Fig. 2) is adapted to support a SCSI disk controller (i.e., SCSI Adapters 220, 222 in Fig. 2).

15. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Peters [US 6,636,927 B1] in view of AAPA as applied to claims 1, 2, 4, 6-9, and 11-14 above, and further in view of Bennett [US 6,510,475 B1].

Referring to claim 10, Peters, as modified by AAPA, discloses all the limitations of the claim 10, except that does not expressly teach that a prefetch size of a memory read multiple command is at least four times as large as said size of a memory read or memory read line command.

Bennett discloses a data fetching control mechanism (See Abstract and Fig. 2), wherein

- a bridge (i.e., P64H 140 of Fig. 1) including a data fetching control mechanism (i.e., CONTROL MEC 146 of Fig. 2), which sets up a prefetch size (e.g., row #8 in Fig. 4, Soft DT Request Length: pre-fetch 8 cache lines) of a memory read multiple command (i.e., cache line size 64

bytes, PCI freq. 66 Mhz, REQ64#-deasserted, and memory read multiple command) is at least four times as large as said size (i.e., row #7 in Fig. 4, Soft DT Request Length: pre-fetch 2 cache lines) of a memory read command (i.e., cache line size 64 bytes, PCI freq. 66 Mhz, REQ64#-deasserted, and memory read command). Refer to col. 7, line 1 through col. 8, line 11.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said data fetching control mechanism, as disclosed by Bell, in said bridge, as disclosed by Peters, as modified by AAPA, for the advantage of providing an efficient data fetching control mechanism which fetches optimized data from a memory subsystem on one side of said bridge (i.e., host bridge such as PCI-PCI bridge) for PCI devices on the other side of said bridge in accordance with characteristics of a particular request, such as a command type, a data width, a clock frequency and a cache line size (See Bennett, col. 2, lines 6-12).

Response to Arguments

16. Applicants' Request for Reconsideration filed on 15th of August 2005 does not have any arguments.

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Batchelor et al. [US 6,490,647 B1] disclose flushing stale data from a PCI bus system read prefetched buffer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on 9:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christopher E. Lee
Examiner
Art Unit 2112

CEL/